REMARKS

Claims 1-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Tanaka et al., U.S. Patent No. 6,489,952. Further, claims 1-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hasegawa et al., U.S. Patent Application No. 2001/0011979. Applicants traverse these rejections because the references do not disclose or suggest a voltage offset to a single positive or negative constant level, as recited in all independent claims 1, 3, 7, 8, 9, 12 and 17.

The present invention prevents decrease of contrast ratio caused by the incomplete memory effect (when data is maintained in a picture element), and in particular, is concerned with preventing light transmittance in the picture element when data pulses of zero amplitude for displaying "black" are applied to the element. The decrease of contrast ratio is prevented by the use of driving signals which are positively or negatively offset a single, predetermined value with respect to a reference voltage of the panel, as shown in Figs. 4D1-4D6, which show potentials appearing across each picture element. The amplitude of the single, offset value is selected depending on a desirable variation of contrast ratio of the display panel (page 14, lines 16-24). The ratio is calculated from the light transmittance factor of black presentation, where the amplitude of the data signal is equal to 0V, and the light transmittance factor at white presentation, where the amplitude of the data signal is equal to 7V. The offset voltage is one constant value, and it can be either a positive or a negative value. In other words, the

offset voltage does not change polarity. Typically, the value of the offset voltage is selected in the range of 0V to 5V for a contrast ratio between 60:1 and 100:1.

In the present invention, the voltage applied to the common electrode 80 is offset a single positive or negative constant level. A common electrode voltage control circuit 6 serves as the controlled offset voltage supplier, which supplies a controlled voltage to the common electrode 80 (page 10, lines 13-18). The voltage ΔVofs is the offset provided to the common electrode 80 for a stable "black" presentation at the screen element (page 11, line 19-23). As seen in FIG. 4C, the voltage ΔVofs is offset from the reference level in the panel 1 by a single, positive constant value. For example, the single, constant offset value may be +2V.

In Tanaka et al., however, at least two offset values are used since the electrode of Tanaka et al. switches potential from negative to positive. Tanaka et al. merely teach two offset values used as part of an inversion driving system, a system in which a direction of an electric field applied to a liquid crystal is inverted at every rewriting of a display screen. In Tanaka et al., a first counter electrode 1 is connected to a potential COM1, and a second counter electrode 2 is connected to a potential COM2. The first and the second counter electrodes 1, 2 do not have the same potential, but have opposite potentials, see FIG. 4. In the first frame scanning period, a negative potential is applied as COM1 at odd source signal lines (S1, S3, S5,...,Sn-1), and a positive potential is applied as COM2 at the even source signal lines (S2, S4, S6,...,Sn). In this way, the potential of the counter electrode has an opposite polarity (+ or -) to the potential of the

image signal applied to the pixel electrode. (Col. 8, lines 47-58) Then, the potential of the counter electrode 1 alternates polarity, for example COM1 switches from a negative potential to a positive potential, which is acknowledged by the Examiner ("The signal line com1 alternates polarity corresponding to when the odd line is driven for display..." Page 2, of Paper 13). For this reason, Tanaka et al. do not disclose or suggest a voltage offset to a single, positive or negative constant level, as recited in the amended claims, because Tanaka et al. disclose two distinct levels, a positive level and a negative level. Withdrawal of this rejection is respectfully requested.

With respect to the Hasegawa et al. reference, the offset voltage is applied to a liquid crystal material during manufacturing or repair of a display, not during operation. In particular, the reference is directed to an alignment treatment for aligning the liquid crystal display, such as when the liquid crystal is destroyed by application of external forces. (paragraph [0088], [0090]). Referring to a sample experiment for an alignment treatment, when a pulse wave was used to apply voltage to the scanning lines, a feedthrough voltage of approximately +1V was generated. The problem of the feedthrough voltage was solved by applying an offset voltage of –1V at the common electrode 17. (paragraph [0117]). Using the offset voltage, "the alignment treatment could be applied and the alignment treatment could be uniformly effected for the entire surface of the image plane...". (paragraph [0118]).

Thus, the offset voltage of Hasegawa et al. is used in the alignment treatment during manufacturing or repair, and not during operation (see paragraph

[0117], [0143]). Figure 4F and 4E show that the voltages are applied during the alignment period, as further seen in Figure 4A. The alignment start signal is output from the alignment controller 36 (paragraph [0090]), and the alignment treatment is processed when the alignment of the liquid crystal is destroyed (paragraph [0088]), therefore the signals shown in Figure 4 do not correspond to an image to be displayed because the liquid crystal has been destroyed. Thus, Hasegawa et al. discloses the treatment process for recovery of the liquid display destroyed and the recovery processing performed only during the alignment period (FIGs. 4 and 2). The present invention, on the other hand, is related to displaying improved images by applying an offset signal during the image display.

Further, all independent claims of the present invention recite features of the display device in terms of structure, or in terms of operation (including, offsetting a voltage). The present invention is not claimed in terms of manufacturing or repairing. For these reasons, withdrawal of this rejection is requested.

For the foregoing reasons, Applicants believe that this case is in condition for allowance, which is respectfully requested. The Examiner should call Applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

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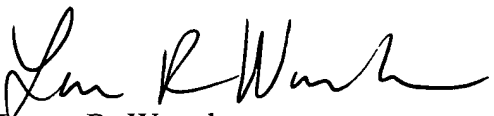
By 
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